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A REVERSIBLE DECIMAL COUNTER

By

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UNEDITED ROUGH DRAFT TRANSLATION

A REVERSIBLE DECIMAL COUNTER

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A REVERSIBLE DECIMAL COUNTER

I. M. Beskrovnyy

Decimal counters consisting of series-connected binary counters, and reversible binary counters are known. A drawback to these known devices is the fact that additional feedback is used in them for reversing, which complicates the device as a whole.

In the device described here this drawback is eliminated by adding two channels to the decimal counter, which consists of four flip-flops with a pair of output channels. The connections between counter cells are made so that there is no need for additional feedback.

The counter contains four flip-flops 1, 2, 3 and 4 (see block diagram), which are connected through channels 5, 6, 7, 8, 9 and 10. At the output of the flip-flop, besides channels 11 and 12, there are additional channels 13 and 14. A subtraction sign is sent to bus 15, and an addition sign to bus 16. The voltage fed to bus 15 controls the uneven channels, and the voltage to bus 16 controls the even channels. Channels 13 and 14 are connected in opposite phase with channels 11 and 12. In addition, signals from the output of channels 11 and 12 enter the unit inputs of flip flops 2 and 3. The

outputs of flip-flop 4 are disconnected: the signal from channels 9 and 10 are sent to one of them, and the signal from channels 5 and 6 are sent to the other.

When summing pulses entering input clip 17, the device retains the ordinary binary code up to the number 7. The eighth pulse switches flip-flops 1, 2 and 3 to the "zero" position, and flip-flop 4 to the "one" position. Thus a binary code of the received number 8 (0001) is set up in the device. However, when flip-flop 4 switches to the "one" position, the current pulse generated at the output of this flip-flop returns flip-flops 2 and 3 to the "one" position through channel 14. The code 0111 is set up in the device, which is taken for the code of the number 8. Accordingly, the combination 1111 is taken as the code for 9 and the combination 0000 is taken for 10.

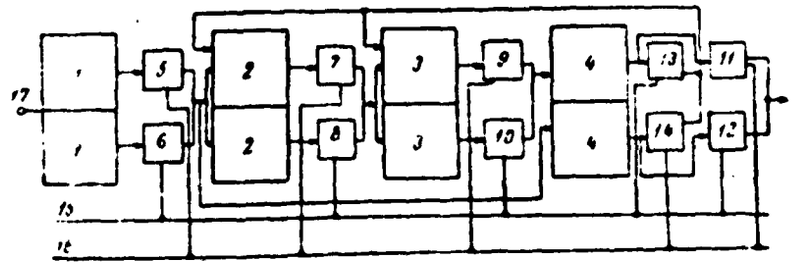
When subtracting pulses entering input clip 17, after the state 0000, the device takes positions 1111 and 0111 successively. These codes, as indicated above, correspond to the numbers 10, 9 and 8.

After this, the output pulse from flip-flop 1 returns flip-flop 4 to the "zero" position. The signal generated at the output of flip-flop 4, through additional channel 13, places flip-flop 2 in the "one" position. The code 1110 is generated in the device, which corresponds to the number 7 in the binary number system. Then the device continues operation as an ordinary binary counter.

Object of the Invention

The reversible decimal counter, consisting of four flip-flops with a pair of output channels, one of which is opened by a "+" signal, and the other by a "-" signal, is distinguished by the fact that, in order to obtain reversing without additional feedback, the fourth flip-flop is connected to an additional pair of gates, and the collected

outputs of the gates are connected to the "one" inputs of the flip-flops of the second and third digits; the "one" input of the fourth digit is connected to the outputs of the channels of the third digit, and the "zero" input to the outputs of the channels of the first digit.



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